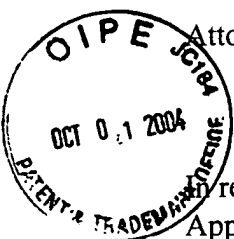


CJC



Attorney Docket No. 5649-888

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Kong et al.

U.S. Patent No.: 6,768,660 B2

Application Serial No.: 09/920,062

Issued: July 27, 2004

Filed: August 1, 2001

For: *Multi-Chip Memory Devices and Modules Including Independent Control of Memory Chips*

Date: September 29, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Certificate  
OCT 0 6 2004  
of Correction

**REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION UNDER  
35 U.S.C §254 AND 37 C.F.R. §1.322**

Sir:

The Assignee of record for the above-referenced patent hereby requests, pursuant to 35 U.S.C §254 and 37 C.F.R. §1.322, that a Certificate of Correction be issued. This request is made in order to correct the mistakes incurred through the fault of the U.S. Patent and Trademark Office. No fee is believed due. However, the Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

The mistakes appearing in the patent are set forth with corrections on the Certificate of Correction enclosed herewith, with an additional copy thereof and a return post card.

Respectfully submitted,

Rohan G. Sabapathypillai  
Registration No. 51,074

Myers Bigel Sibley & Sajovec, P.A.  
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Customer No. 20792

**Certificate of Mailing under 37 CFR 1.8**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 29, 2004.

Monica L. Croom

OCT 0 8 2004

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,768,660 *B2*  
DATED : July 27, 2004  
INVENTOR(S) : Kong et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

Column 11, line 17 should read -- corresponding data pads of each of the integrated circuit --

Column 11, line 51 should read -- which includes a plurality of corresponding address --

Column 12, line 7 should read -- **12.** A memory module according to claim **11** wherein the at least --

Column 12, line 32 should read -- **16.** A memory module according to claim **11** wherein the --

Column 12, line 58 should read -- external system clock signal to the at least two integrated --

MAILING ADDRESS OF SENDER:  
Myers, Bigel, Sibley & Sajovec  
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PATENT NO. 6,768,660 *B2*  
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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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